Zhang et al. EURASIP Journal on Embedded Systems (2018) 2018:1
https://doi.org/10.1186/s13639-018-0085-2

EURASIP Journal on Embedded Systems

RESEARCH Open Access

A new test set compression scheme for circular scan

Ling Zhang*, Junjin Mei and Bowu Yan

Abstract

A new test data compression scheme for circular scan is proposed in this paper. For circular scan, the response of the previous test vector is used as the next test vector's template, and only the conflicting bits between the previous response and the next vector are required to be updated. To reduce the test data volume and test application time, the problem addressed here is minimizing the number of conflicting bits by optimally reordering test vectors. Each vector represents a city, and the number of conflicting bits between two test vectors is regarded as the distance between them. Thus, the problem corresponds to the travelling salesman problem (TSP), which is NP-complete. The genetic algorithm is used to solve this problem. The experimental results show that the proposed scheme could reduce the test data volume efficiently without any additional hardware cost.

Keywords: Built-in self-test (BIST), Test application time, Fault coverage

1 Introduction

The large size of test data volume is one of the major challenges for complex circuits, and the problem is aggravated by the scale increasing [1]. Continued advances in process technology have led to a relentless increase in the design complexity of integrated circuits (ICs). Besides the increased density, the need to test new types of defects in nanometer technologies also results in a tremendous increase in the test data volume and test application time [2, 3]. High-test data volume may exceed the limited memory depth of the automatic test equipment (ATE).

One of the most effective schemes for reducing test data volume is test data compression, where test data provided by the vendor are stored in the memory of a tester, and an on-chip decoder is used to apply the corresponding test vectors to circuits under test (CUT). Many test compression schemes have been proposed in recent decades, and they can be classified into three categories: code-based compression scheme [4, 5], linear decompression-based scheme [6, 7], and broadcast-scan-based scheme [8, 9]. Code-based compression schemes encode for pre-computed test data; linear decompression-based schemes use a linear decompression module to apply test data to CUTs; and broadcast-scan-based schemes broadcast identical test data to multiple scan cells at the same time. These test compression schemes are all based on the conventional scan architecture.

Circular scan architecture (CSA) [10] is another effective design for testing (DFT) architecture, and it has a comparable hardware with a conventional scan. The affirmative attribute of the CSA is that the response of previous test patterns could be used as the next pattern's template, which makes test data compression easier.

The circular scan scheme was first proposed in paper [10] as a BIST scheme without using any storage. Then, several schemes for reducing the test cost were proposed, and they can be classified into two types: *self-testing using circular scan* [10–13] and *determining-testing using circular scan* [14–17].

For self-testing using circular scan, circular scan serves as the test pattern generator and the test response compactor. It operates random testing for sequential logic circuits, where parts of flip-flops are selected as the scan cells. In determining-testing using circular scan, circular scan is used as a DFT architecture, and the pre-computed test data can be easily applied to it. Paper [14] first used circular scan to determine the test architecture, where the previously captured response was used as the next test pattern template, and the captured response can be fully observed without any fault coverage loss. To reduce the

* Correspondence: forry1230@126.com
School of Computer, Hubei Polytechnic University, Huangshi 435003, China

test data volume further, many works have been proposed to optimize the CSA.

Papers [14, 15] addressed the conflicting bits between the template and test pattern. Paper [16] proposed a modified circular scan where multiple circular scan chains are used to test circuits under testing (CUT). Paper [17] proposed a new test compression scheme based on circular scan, where multiple conflicting bits are updated through inputs of the scan chains that use a multiple-hot decoder.

The key point of determining circular scan's compression is minimizing the number of conflicting bits between the template pattern and the real test pattern. To reduce test data volume, this paper proposes a new test vector reordering scheme where the minimizing problem can establish the corresponding travelling salesman problem (TSP), which is NP-complete. We use the genetic algorithm to solve this problem.

2 The conflicting bit minimization for circular scan

Figure 1 shows the architecture of the circular scan [15]. As shown in the figure, the previous captured response is a template of the next pattern, and the content of scan cells could be updated by multiple rotations of scan chains. To reduce the test application time, the multiplexer-based decoder is used to change the test data concurrently. *One-bit-update mode* and *broadcast mode* are designed to load the next determined test pattern to reduce test data volume. The fewer bits there are that need to be updated, the smaller the test data volume is. So, the critical problem of the circular scan is minimizing the number of conflicting bits between the template and the real test pattern.

Figure 2 gives an example of an application of the circular scan. As shown in the figure, three scan chains with eight scan cells each are contained in the example circuit under test (CUT). The corresponding test set is given in Table 1. There are five test patterns denoted as $V1$, $V2$, $V3$, $V4$, and $V5$. The corresponding responses represented as $R1$, $R2$, $R3$, $R4$, and $R5$ are also given in the table. To achieve the test mode of circular scan, in that the previous response is used as the next pattern's template, the conflicting bits between them should be updated. If $V2$ is the first test vector applied, then the corresponding response $R2$, $V3$ is used. The number of conflicting bits between $R2$ and $V3$ that are computed for their hamming distance is 13 bits. On the other hand, if $V3$ is used first, followed by $V2$, then only 10 conflicting bits need to be updated. To reduce test data volume, the conflicting bits should be minimized.

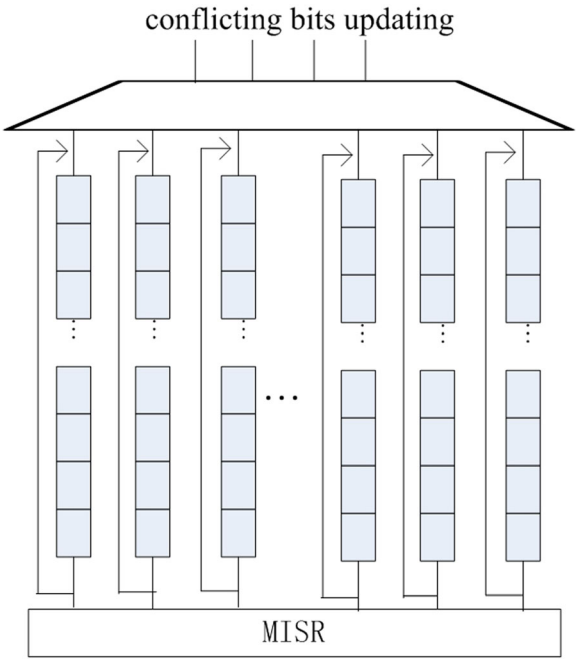

Fig. 1 The architecture of the circular scan

To solve this problem, the test set weight matrix and the corresponding weight illustration for Table 1 are given in Fig. 3a, b, respectively. As shown in Fig. 3b, each vertex represents a test pattern, and the number of conflicting bits between the response of vi and the pattern of vj that was computed as the hamming distance between the two is denoted as the weight of the edge. It is obviously a directed graph. Different orders of the test patterns will result in a different number of conflicting bits. For example, the order of $V1$, $V2$, $V3$, $V4$, and $V5$ has the number of conflicting bits $W12 + W23 + W34 + W45 = 8 + 13 + 5 + 9 = 35$, where Wij denotes the weight of the two vertexes of i and j. The order of $V2$, $V1$, $V5$, $V4$, and $V3$ gains the number of conflicting bits as $W21 + W15 + W54 + W43 = 8 + 6 + 12 + 5 = 31$, which has a smaller number of conflicting bits. The order of the test patterns influences the number of conflicting bits that need to be updated, and that number should be minimized.

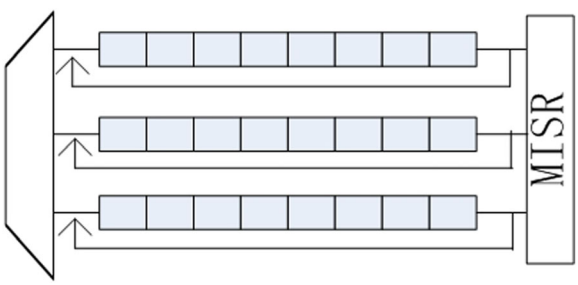

Fig. 2 An example of circular scan

Table 1 The example test sets for circular scan

Vectors		Responses	
V1	1x00 x00x 0xxx 1001 010x x010	R1	0011 1111 0101 1101 1010 0000
V2	0x10 0x10 011x 1xx1 00x0 11x1	R2	0010 1101 1111 1111 0010 0000
V3	00xx 0010 xx11 0000 1101 0010	R3	1100 1111 0000 1101 1111 1110
V4	xx00 1011 xxxx 0101 1000 xxxx	R4	0101 0010 1111 0010 1111 1101
V5	0000 xxxx 1101 1111 0000 00xx	R5	0101 0000 1101 0000 1111 1111

The problem is an *NP*-complete problem in reality. Note: Let the number of test patterns be n. The weights of each of the two patterns are easily obtained by computing their hamming distance, and the weights of two vertexes of Vi and Vj are denoted as Wij and Wji, respectively. The problem is finding the shortest path that passes through every vertex once and only once. So, the problem can be transformed and formally stated as follows.

2.1 Problem 1

Given a directed graph with n vertexes, the distance between each of the two vertexes can be computed. Find the shortest path traveling across each vertex once and only once.

Problem 1 is equivalent to the well-known travelling salesman problem (TSP) [18], which is NP-complete, where the vertexes stand for towns and the number of conflicting bits between every two vertexes represents the distance between two towns.

To solve the problem of the conflicting bits minimizing problem, which is NP-completed, the genetic algorithm (GA) is used in the paper. The GA is one of the mature techniques for solving the TSP problem. The objective of the GA is to determine the surviving individuals, the reproducing individuals, and the ones that died. GALIB [19] is an effective genetic tool to solve several NP-completed problems, specifically the ones corresponding to the TSP. GALIB was selected for solving the conflicting bits minimizing problem in the paper. The result of the example in Fig. 3a and Table 1 using GALIB is given in Fig. 3c. The optimizing order of the five vectors is $v2 \rightarrow v5 \rightarrow v3 \rightarrow v1 \rightarrow v4$, and the number of corresponding conflicting bits that need to be updated is 21 bits. Compared to that of the primary order $v1 \rightarrow v2 \rightarrow v3 \rightarrow v4 \rightarrow v5$ of 35 bits, 14 bits are reduced.

3 Experimental results

Five of the largest ISCAS'89 circuits and ITC'99 circuits are used in the experiments. The Atalanta [20] tool is used to generate the test sets. The TSP solver [19] is used to minimize the conflicting bits for the circular scan. The experimental results are given in Tables 2, 3, and 4.

Table 2 shows the test volume compression ratio comparison with related schemes. The compression ratio is computed as $CR = (T_D - T_E)/T_D$, where T_D is the test data volume of the primary test sets and T_E is the test data volume of the compressed test sets. The first and second columns denote the names of the circuits and the numbers of the flip-flops. The number of scan chains is represented as #SC. The compression ratio of the proposed

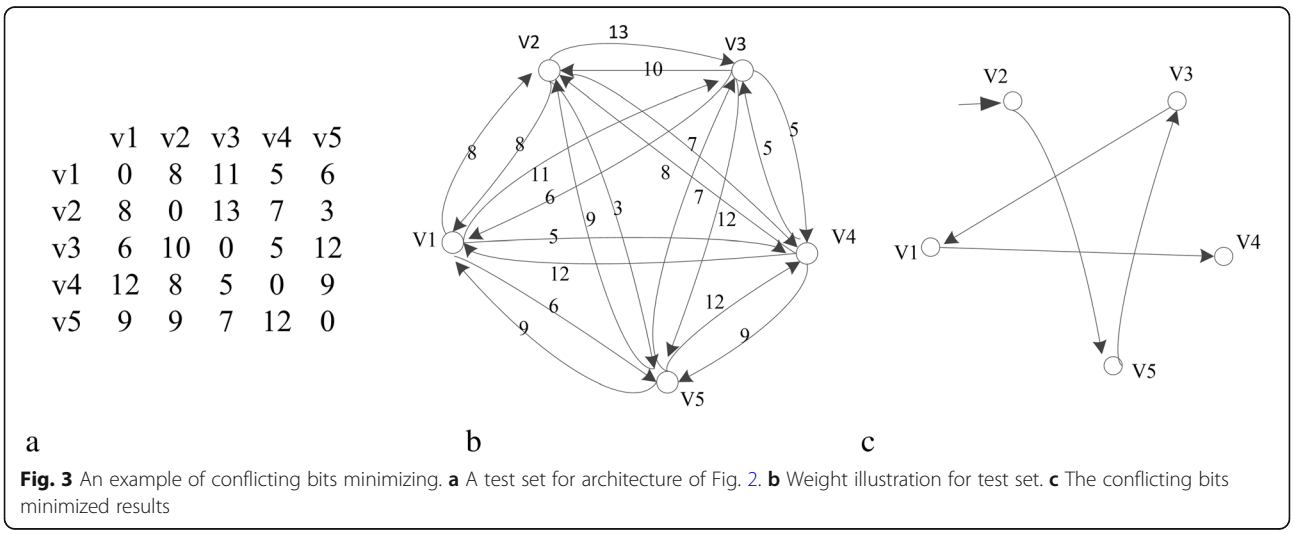

Fig. 3 An example of conflicting bits minimizing. **a** A test set for architecture of Fig. 2. **b** Weight illustration for test set. **c** The conflicting bits minimized results

Table 2 Test volume compression ratio comparison results

Circuits	#ff	#SC = 64			#SC = 128				#SC = 256			
		[14]	[16]	[17]	Pro.	[14]	[16]	[17]	Pro.	[14]	[16]	[17]	Pro.
s13207	669	53.6	58.3	68.4	71.4	65.1	67.8	77.3	79.6	61.6	69.3	79.4	81.4
s15850	597	28.9	33.7	45.5	47.7	39.5	44.5	62.1	63.0	44.2	51.6	63.1	64.2
S35932	1728	5.1	7.2	33.3	36.2	16.2	20.1	66.4	67.7	21.7	26.0	75.3	76.4
s38417	1636	28.3	32.6	48.1	51.1	36.8	42.9	59.2	61.5	42.2	48.3	59.7	61.9
s38584	1452	30.9	35.4	51.5	54.7	40.7	48.1	60.3	62.8	48.9	55.6	71.8	73.5

scheme is expressed as *Pro*. As shown in Table 2, for different scan chains *#SC* = 64, *#SC* = 128, and *#SC* = 256, the proposed scheme minimizing the conflicting bits that need to be updated achieves a better compression ratio in all cases.

The test application time comparison is given in Table 3. The first and second columns also represent the circuit names and the number of flip-flops, while *#SC* is the number of scan chains. Paper [16] proposed a scan input selection unit that updates conflicting bits internally and eliminates loading conflicting bits from ATE, so only the test data volume is reduced, and it has the same test application time as paper [14]. Thus, the test application time of paper [14] and paper [17] are compared with our method. As shown in the table, because the number of test data that needed to be updated was reduced, the test application time was also reduced compared with the other related solutions, in all cases.

Except the comparison with other related works using the five biggest ISCAS'89 benchmark circuits. We also gathered experimental results on ITC'99 circuits. The results are given in Table 4. As shown in the table, the first and second columns are the circuits and the number of flip-flops, CR represents test compression ratio, and TT is the test application time. *Ord* is the test patterns generated by the ATPG (automatic test pattern generation) tool of Atalanta [20] before using the proposed scheme, and *Pro* is the new test patterns with new orders that under the proposed optimized schemes. Because the proposed scheme reordered test patterns which made the number of conflicting bits minimized, it achieves better test compression ratios and test application times in all cases.

Table 3 Test application time comparison results

Circuits	#ff	#SC = 64			#SC = 128			#SC = 256		
		[14]	[17]	Pro.	[14]	[17]	Pro.	[14]	[17]	Pro.
s13207	669	51.2	70.3	72.62	64.1	73.7	74.68	66.2	80.3	82.65
s15850	597	31.5	50.6	53.76	38.0	65.4	65.95	43.8	67.1	68.09
s25932	1728	9.6	44.7	46.32	15.1	68.9	70.35	17.8	72.5	74.07
s38417	1636	30.3	50.6	53.70	35.8	56.4	58.61	43.4	63.2	65.61
s38417	1452	31.7	59.4	60.82	43.3	65.1	66.03	51.6	73.6	75.14

From these tables, we could see that through the proposed scheme, the number of conflicting bits needed to be updated was minimized, so the corresponding test data volume and test application time were both reduced in all cases.

Furthermore, we could also see that the compression ratio and the test application time reduction were different for different circuits. This is because for different circuits, the corresponding test set has different 0, 1, and X (denotes the do not care bits that can be set as 0 or 1) distributions. For those circuits with more Xs and more compatible bits (two bits have identical data or one of X), the corresponding number of conflicting bits is smaller, so the bits that need to be updated are fewer, which would reduce the test data volume and test application time. On the other hand, for those circuits with very few Xs and compatible bits, more data bits need to be updated, and the corresponding data volume and test application time reduction achieved were less.

For example, for the circuit S35932, the corresponding conflicting bits between the previous response and next pattern are more, so the test data volume and test application time reductions are both smaller compared with other circuits. Nevertheless, the circuit of 13,207 has more Xs, and the number of conflicting bits is very small, so it attained a higher reduction in test data volume and test application time.

4 Conclusions

To reduce the test data volume and test application time, this paper proposes a new test data compression scheme for circular scan, where the response of the previous pattern is used as the next pattern's template. To reduce the conflicting bits that needed to be updated, the conflicting bit minimization problem can establish the correspondence with the travelling salesman problem, which is NP-complete. The genetic algorithm is used to solve this problem in this paper. The experimental results show that the average compression ratio is improved about 3.97% compared

Table 4 Experimental results on ITC'99

BM	#ff	#SC = 64				#SC = 128				#SC = 256			
		CR		TT		CR		TT		CR		TT	
		Ord	Pro.	Ord	Pro.	Ord	Pro.	Ord	Pro.	Ord	Pro.	Ord	Pro.
b14	245	40.32	44.37	38.7	42.1	44.8	47.0	45.0	48.2	41.6	52.3	41.6	45.3
b15	449	25.6	27.9	28.3	30.6	31.6	41.2	33.5	43.7	27.1	35.1	28.0	31.3
b17	1415	9.9	15.6	13.2	15.8	12.7	20.7	16.3	25.9	10.9	21.1	12.3	15.6
b20	490	20.8	23.8	22.9	25.4	25.7	29.9	24.7	28.0	22.7	33.6	24.9	27.2
b21	490	20.4	31.0	20.5	23.7	26.3	32.5	26.2	35.4	21.6	32.9	23.2	24.8
b22	735	23.2	33.9	25.1	27.0	27.1	35.4	29.6	36.1	25.7	32.4	26.8	28.1

with paper [17], improved about 34.28% compared with paper [16], and improved about 42.51% compared with paper [14]. For circuit of S13207 in the case of #SC = 256, the compression ratio is as high as 81.4. We could see that the proposed scheme could efficiently reduce test data volume and test application time for circular scan.

Funding
The research work was supported by the Natural Science Foundation of China (no. 61472123), the Scientific Research Project of Hubei Province Department of Education (no. D20174501), and the Outstanding Youth Science and Technology Innovation Team Project of Hubei Polytechnic University (no. 13xtz10).

Availability of data and materials
Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

Authors' contributions
Author LZ gave the idea of the paper and made experiments with author JM and author BY. All the authors had taken part in the manuscript written. All authors read and approved the final manuscript.

Ethics approval and consent to participate
Not applicable

Consent for publication
Not applicable

Competing interests
The authors declare that they have no competing interests.

Publisher's Note

Received: 14 January 2017 Accepted: 15 June 2018
Published online: 03 July 2018

References

1. Filipek, M, et al. (2015). Low-power programmable PRPG with test compression capabilities. *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, *23*, 1063–1076.
2. Lee, DH, & Han, TH (2014). An improvement technique for the test compression ratio and application time of multiple expansion scan chain based SoC using new cost function. In *IEEE 57th International Midwest Symposium on Circuits and Systems: 3–6, Aug*, (pp. 129–132). College Station: IEEE.
3. Li, Z, Jonathon, EC, Pagalone, V, Narayanun, K, Chakrabarty, K (2017). Test-cost optimization in a scan-compression architecture using support-vector regression. In *IEEE 35th VLSI Test Symposium, Las 18 Ma*, (pp. 1–6). Vegas: IEEE.
4. Kavousianos, X, Kalligeros, E, Nikolos, D. (2008). Multilevel-Huffman test-data compression for IP cores with multiple scan chains. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, *16*, 926–931.
5. Muthyala, SS, & Touba, NA (2012). Improving test compression by retaining non-pivot free variables in sequential linear decompressors. In *IEEE International Test Conferenc, 5–8, Nov*, (pp. 1–7). Anaheim; New York: IEEE.
6. Lee, T, Toub, NA, Yang, J-S. (2017). Enhancing test compression with dependency analysis for multiple expansion ratios. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, *36*, 1571–1579.
7. Jia Li, Yu Huang, Dong Xiang, Prediction of compression bound and optimization of compression architecture for linear decompression-based schemes. IEEE 29th VLSI Test Symposium, May 2011, Dana Point: IEEE. pp. 297–302.
8. Chen, J-Z, & Lee, K-J. (2017). Test stimulus compression based on broadcast scan with one single input. *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, *36*, 184–197.
9. Banerjee, S, Mathew, J, Pradhan, DK, Mohanty, SP (2010). Layout-aware Illinois scan design for high fault coverage. In *International symposium on quality electronic design: 22–24 Mar*, (pp. 683–687). San Jose: IEEE.
10. Pradhan, MM, Brien, EJO, Lam, SL, Beausang, J (1988). Circular BIST with partial scan. In *International Test Conference*, (pp. 719–729). Washington, DC: IEEE Piscataway, NJ, United States.
11. Krasniewski, A, & Pilarsk, S. (1989). Circular self-test path: a low-cost BIST technique for VLSI circuits. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, *8*, 46–54.
12. Krasniewski, A, & Pilarski, S (1987). Circular self-test path: a low-cost BIST technique. In *Proc. IEEE Des, Auto. Conf.*, (pp. 407–415). Miami Beach: EEE New York, NY, USA.
13. Touba, NA. (2002). Circular BIST with state skipping. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, *10*, 668–672.
14. Arslan, B, & Orailoglu, A (2004). Circular Scan: A scan architecture for test cost reduction. In *Design, automation and test in Europe conference and exhibition*, (pp. 1290–1295). Paris: IEEE.
15. Arslan, B, & Orailoglu, A (2004). Design space exploration for aggressive test cost reduction in circular scan architectures. In *International Conference on Computer-Aided Design*, (pp. 726–731). San Jose: Institute of Electrical and Electronics Engineers Inc (IEEE).
16. Azimopour, M, Eshghi, M, Khademzadh, A (2007). A modification to circular-scan architecture to improve test data compression. In *International conference on advanced computing and communications*, (pp. 27–32). Guwahati: Institute of Electrical and Electronics Engineers Inc.
17. Azimipour, M, Fathiyan, A, Eshghi, M (2008). A parallel circular-scan architecture using multiple-hot decorder. In *15th International Conference on Mixed Design*, (pp. 475–480). Poznan: Inst. of Elec. and Elec. Eng. Computer Society.
18. Lawler, EL, Lenstra, JK, RinnooyKan, AHG, Shmoys, DB (1985). *The traveling salesman problem*. Chichester: Wiley.
19. A C++ genetic algorithm library: http://lancet.mit.edu/galib-2.4/, 2018.2.
20. Lee, HK, & Ha, DS (1993). *Atalanta: an efficient ATPG for combinational circuits, technical report*. Blacksburg, Virginia: Dep't of Electrical Eng., Virginia Polytechnic Institute and State University.