Hindawi Publishing Corporation
EURASIP Journal on Embedded Systems
Volume 2010, Article ID 641261, 2 pages
doi:10.1155/2010/641261

Editorial

Design Methodologies and Innovative Architectures for Mixed-Signal Embedded Systems

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Received 18 February 2010; Accepted 18 February 2010

The continuous evolution of VLSI technologies, especially CMOS and its variants (HV MOS, BCD, RF CMOS, etc.), has enabled the integration of complex functionalities in a single, heterogeneous embedded system. Digital subsystems, such as microprocessors, memories, or communication interfaces, can be integrated onto the same substrate (System-on-Chip) or the same package (System-in-Package) together with RF blocks, analog acquisition and processing circuits, analog power drivers, and even micromechanical parts for sensors and actuators.

Overcoming the classic dichotomy between analog and digital domains, such new generation of mixed-signal embedded systems is fueling the development of more efficient and performance solutions in several technology areas, to name just a few, distributed control-sensing-actuation units to increase safety, comfort, and engine efficiency in vehicles, software defined and cognitive radios for multimode multimedia communication, wireless sensor networks for ambient intelligence in home, industrial scenarios, or for environment control.

The opportunity given by mixed-signal embedded systems comes, however, with lots of challenges. Assembly and integration of heterogeneous blocks onto the same chip or the same package is already a big technological challenge. However, these systems also bring with them several design challenges. At different levels of the design flow, innovative methods, computer-aided design (CAD) tools, as well as architecture and circuit techniques need to be developed to allow successful design of mixed-signal integrated systems. Codesign of the different subsystems, hardware and software but also RF/analog with digital and power, has become instrumental to achieve high performance at reasonable costs. However, system-level specification, simulation, and optimal hardware/software, analog/digital partitioning are still open research fields. Moreover, whenever the largest payoffs in design originate from system level optimization, implementing hardware building blocks with increased flexibility and programmability becomes a wanting to enable intellectual property (IP) block sharing and reuse. Finally, efficient and reliable verification and testing strategies need to be devised, by leveraging a combination of simulation, formal methods, and rapid prototyping.

This special issue, including 7 papers from both Europe and America, will give to the readers an overview of the ongoing research in academia and industry in the field of design methodologies and architectures for mixed-signal systems. In particular, the papers address several case studies in automotive, consumer electronics, and wireless communication, demonstrating how the realization of mixed-signal embedded systems can either enable new services and applications or improve performance, efficiency, and cost of the existing ones.

The first two papers deal with design methodologies. The first paper "A platform-based methodology for system-level mixed-signal design," by the University of California at Berkeley and Marvell Inc., presents a system-level design methodology for electronic circuits, utilizing the platform-based design (PBD) paradigm as the natural framework for mixed-domain design formalization. In PBD, a meet-in-the-middle approach allows systematic exploration of the design space through a series of top-down mapping of system constraints onto component feasibility models in a platform

library, which is based on bottom-up characterization of the design components. A robust optimization scheme is proposed to account for modeling errors as well as process, voltage, and temperature variations. In this framework, new designs can be assembled from the precharacterized library components, giving the highest priority to design reuse, correct assembly, and efficient design flow from specifications to implementation. The effectiveness of the PBD methodology is demonstrated on the design of a pipeline A/D converter and two receiver front-ends, for UMTS and UWB communications, in submicron CMOS technologies.

The second paper "On mixed abstraction, languages and simulation approach to refinement with systemC AMS" by the University of Vienna proposes a methodology based on SystemC-AMS to be applied to complex mixed-signal embedded systems in performing early design decision trade-off exploration, architecture experimentation, and, particularly, model refinement and critical behavior analysis. An RTL model of a data encryption standard is demonstrated as an example.

The third paper "Systematic development methodology for mixed-mode behavioral models of in-vehicle embedded electronic systems," by the Universities of Genoa and Santa Catarina (Florianopolis, Brazil) and On Semicondutors, presents a systematic development methodology for mixed-mode behavioral models of automotive embedded systems, with particular reference to in-vehicle networks. The methodology allows achieving accurate models, which provide reliable system simulations. Two automotive case studies are presented concerning a Flexray physical layer transceiver and a CAN bus transceiver-integrated circuit. Thanks to the increased simulation speed and flexibility with respect to transistor level modeling techniques, fast communication network design, modification, and verification are permitted.

Automotive applications are also the focus of the following two papers, proposing innovative mixed-signal architectures for multisensor signal conditioning and piezoelectric actuator driving. The paper "A mixed-signal embedded platform for automotive sensor conditioning," from the University of Pisa and SensorDynamics AG, presents the Intelligent Sensor InterFace (ISIF) system, a mixed signal system able to fast identify, trim, and verify sensor interfaces. The system, developed according to a platform-based design approach, consists in a set of optimized high-performance analog, digital, and software IP modules that can interface to several kinds of sensors. These IPs can be easily defined for fast prototyping of the interface circuit of a given sensor. Final ASIC implementation of the desired conditioning circuitry can then be easily derived with reduced risk and short development time. Several case examples of sensor conditioning (rate-gyro, magnetic angular position, low-g accelerometer) are presented to demonstrate the effectiveness and flexibility of this system.

In the paper "Model and design of a power driver for piezoelectric satack actuators," from the Polytechnic of Turin, a power driver has been developed to control piezoelectric stack actuators used in automotive application. An FEM model of the actuator has been implemented starting from experimental characterization of the stack and mechanical and piezoelectric parameters. Experimental results are reported to show a correct piezoelectric actuator driving method and the possibility to obtain a sensorless positioning control.

Architectures for consumer electronics, both audio and wireless communications are presented in the last two papers. In "Mixed-signal architectures for high efficiency and low distortion digital audio processing and power amplification," from the University of Pisa, the algorithmic and architectural design of digital input power audio amplifiers is addressed. A modeling platform, based on a meet-in-the-middle approach between top-down and bottom-up strategies, allows a fast but still accurate exploration of the mixed-signal design space. Different amplifier architectures are configured and compared to find optimal trade-offs among different cost-functions: low distortion, high efficiency, low circuit complexity, and low sensitivity to parameter changes. A novel amplifier architecture is derived; its prototype targeting power levels of tens of Watts implements digital processing IP macrocells on a single low-complexity FPGA while off-chip components are used only for the power output stage (LC filter and power MOS bridge), and no heatsink is required. Discussions towards the full-silicon integration of the mixed-signal amplifier in embedded devices, by using a BCD technology and targeting power levels of a few Watts, are also reported.

We conclude with a paper on Phase-Locked Loop (PLL) design. PLLs are an essential component in many wireline and wireless applications for clocking and frequency synthesis. Moreover, PLL is among those building blocks that mostly took advantage of CMOS scaling and the integration of digital logic with analog circuits. The paper "AD-PLL for WiMAX with digital bang-bang TDC and glitch correction logic", from the Polytechnic of Milan, describes the design of an All-Digital Phase-Locked Loop (ADPLL) in 90 nm CMOS for WiMAX wireless applications. In the proposed architecture a time-to-digital converter (TDC) is implemented as a delay-locked loop (DLL) to be insensitive to process spreads and it uses a lead-lag phase detector and a digital loop filter to further take advantage of the digital approach. A glitch-corrector logic is also described to remove spurs due to time skew between counter and TDC, thus allowing to meet the phase noise specifications.

We hope that this special issue will provide the readers with a good understanding of ongoing research in both academia and industry and of the challenges on the road ahead.

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