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Editorial

Field-Programmable Gate Arrays in Embedded Systems

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Welcome to the special issue on field programmable gate arrays (FPGAs). FPGAs are becoming an increasingly important part of embedded systems, as the collection of papers in this issue illustrates.

"An overview of reconfigurable hardware in embedded systems" provides a comprehensive overview of the state-of-the-art use of reconfigurable hardware in embedded systems. A detailed discussion of the use of FPGAs for application areas such as encryption, software-defined radio, and robotics is provided. Additionally, a concise assessment of design issues and current design tools is included. A sizable collection of citations provides a handy reference for newcomers to the field.

The remaining papers address applications and tools for embedded systems design. The applications presented here are typical of the spectrum of FPGA applications. They fall into the categories of multimedia processing, including video, image and speech processing, as well as communications applications.

The implementation of an MPEG-4 image encoder using a scalable number of Altera NIOS soft processors is presented in "Scalable MPEG-4 encoder of FPGA multiprocessor SOC." An image is partitioned so that each processor receives a horizontal slice of the image. The author's own on-chip interconnection network is used to connect the soft processors. The authors demonstrate a significant application speedup as additional soft processors are added to the FPGA platform.

In "A real-time wavelet domain video denoising implementation in FPGA," the authors present a two-FPGA solution for performing video denoising via a 3D (two spatial and one temporal dimension) wavelet filter. By careful consideration of the algorithm, data movement, and pipelining, a complete and complex image processing pipeline is produced.

In "A dynamic reconfigurable hardware/software architecture for object tracking in video streams," the authors present a feature tracker that has been implemented on an FPGA. The authors focus on choosing an algorithm that is well matched to reconfigurable hardware, hardware/software partitioning, and efficient use of memory structures. Their implementation, which runs faster than a software-only solution, has applications for mobile autonomous platforms.

The paper "Speech silicon: an FPGA architecture for real-time hidden Markov model-based speech recognition" details the implementation of an FPGA SoC that can perform real-time speech recognition of medium-sized speech vocabularies. This pipelined approach maximizes the throughput by minimizing the amount of required control circuitry. The FPGA implementation of each part of the pipeline is carefully documented to demonstrate the benefits of FPGA specialization. FPGA floorplanning plays an important role in achieving real-time performance.

A common application for FPGAs is image processing algorithms. In "A visual environment for real-time image processing in hardware (VERTIPH)," the authors propose a new tool for designing image processing implementations on FPGAs. The proposed tool aims to improve the productivity of designers targeting FPGAs for their image processing algorithms, and provides visual information for the timing and structure of the implementation.

In "FPGA-based communications receivers for smart antenna array embedded systems," the authors consider the design of adaptive receivers on FPGAs. The receivers can support an array of antennas, and make use of adaptive algorithms to change parameters depending on the environment. This approach is particularly good at reducing the power required to receive signals.

An interesting aspect of embedded systems using FPGAs is the use of both CPUs and reconfigurable logic in the same

system; and two papers in this issue address tools for supporting hardware/software codesign.

The first paper is "Modeling and design of fault-tolerant and self-adaptive reconfigurable networked embedded systems." In traditional mixed hardware/software systems, the designer picks which resources will support which tasks. In this paper, the authors explore a different approach—dynamic movement between these resources. This paper describes a framework for implementing a fault-tolerant system containing FPGAs and processors. Tasks can be dynamically bound to hardware or software, and support for checkpointing and rollback is provided.

"MOCDEX: multiprocessor on-chip multiobjective design space exploration with direct execution" supports the design of multiprocessor systems on a chip. The processors here are MicroBlaze soft-cores on a Xilinx Virtex chip. Four are used to implement an image filtering application. The contribution of this paper is in the use of a multiobjective evolutionary algorithm to optimize the design of each processor. The optimization criteria chosen are number of logic slices, amount of block RAM and number of cycles. Real FPGA implementations are used in the evaluation phase of the algorithm.

Another important aspect of tools for embedded systems is energy estimation and power minimization. Two papers in this issue address this problem. "Rapid energy estimation for hardware-software codesign using FPGAs" outlines the design and implementation of a high-level energy estimation approach for combined hardware/software designs mapped to FPGAs. The FPGA design includes both a soft processor and custom application hardware. Cosimulation of the hardware and software is performed to determine software instruction usage and hardware switching activities. This information is then used by low-level instruction-level and hardware models to estimate energy consumption. A 6000x speedup in energy estimation time is achieved versus synthesis-based approaches with a loss of about 10% energy estimation accuracy.

Power consumption in an embedded system is often the crucial design constraint. Although research efforts have developed CAD algorithms to replace vendor tools to perform power optimization, real designers are still reliant on the vendor's tools. The paper "FPGA dynamic power minimization through placement and routing constraints" takes a different track, showing that by carefully devising placement constraints, power reductions in a Xilinx FPGA are possible within the vendor's tool suite. A number of schemes for devising these placement constraints are considered, and overall achieve approximately a 10% power savings.

This collection of papers represents a good overview of active research in the field of reconfigurable hardware in embedded systems. We hope you enjoy this special issue.

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Miriam Leeser is a Professor at Northeastern University, Department of Electrical and Computer Engineering. She received her B.S. degree in electrical engineering from Cornell University, and Diploma and Ph.D. degrees in computer science from Cambridge University in England. After completion of her Ph.D., she joined the faculty of Cornell University, Department of Electrical Engineering, as an Assistant Professor. In January, 1996 she joined the faculty of Northeastern University, where she is the Head of the Reconfigurable Computing Laboratory and a Member of the Computer Engineering Research Group and the Center for Communications and Digital Signal Processing. In 1992 she received an NSF Young Investigator Award to conduct research into floating-point arithmetic. Her research interests include hardware description languages, high-level synthesis, computer arithmetic, and reconfigurable computing for signal and image processing applications. She is a Senior Member of the IEEE, and a Member of the ACM.

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