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Editorial
Dynamically Reconfigurable Architectures

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As integrated circuit line widths continue to shrink, there is a corresponding increase in the capital costs of microelectronic fabrication plants and in the mask making costs of individual chips. As a result, it is increasingly uneconomical to produce small and medium volume chips in the latest submicron technologies. Reconfigurable logic circuits, such as FPGAs (field programmable gate arrays) and coarse-grained processor arrays, allow a single mask-level design to be configured for many different applications, so improving the production volumes and economic viability of the mask-level design.

However, configurability comes at a cost—the area of a configurable circuit is often larger, the power consumption is greater, and the speed is slower than a full-custom circuit. Such configurable circuits become much more attractive if the same logic substrate can be reconfigured and reused for different functions during different phases of an application. Such systems, where the configurable circuit structures are changed during circuit operation, are called dynamically reconfigurable architectures.

In April 2006, the fourth workshop in a series of workshops on the topic of dynamically reconfigurable architectures (DRAs) was held at the *Internationales Begegnungs- und Forschungszentrum für Informatik* (International Conference and Research Center for Computer Science) at Schloss Dagstuhl in Germany. The workshop attendees were invited to submit extended versions of their workshop presentations for consideration for this special issue, and after a peer review process, seven papers were accepted for publication.

The workshop provided participants with an opportunity to review the history of DRAs, to present a summary of their current work, and to explore the challenges and opportunities that these architectures will present in the future. These seven papers in the special issue reflect this diversity. Some papers present a consolidated summary of a large body of work, others look at technologies that will support future generations of reconfigurable circuits.

One of the key problems in DRAs is how to design circuit components that can be swapped in and out of a system. In the first paper, "Prerouted FPGA cores for rapid system construction in a dynamic reconfigurable system," T. Oliver and D. Maskell look at how to build FPGA-based processing cores suitable for use in DRAs. In the second paper, "Efficient integration of pipelined IP blocks into automatically compiled datapaths," Andreas Koch looks at how to combine manually optimised IP blocks with automatically compiled modules.

Another area of active interest in DRAs is identification of suitable application domains in which dynamic reconfiguration can be used to advantage. In the third paper, "Using simulated partial dynamic run time reconfiguration to share embedded FPGA compute and power resources across a swarm of unpiloted airborne vehicles," D. Kearney and M. Jasiunas investigate how dynamic reconfiguration can be used to move computations within a cooperating cluster of autonomous vehicles so as to make best use of available electrical energy and available computing power. In the fourth paper, "Efficient architectures for streaming DSP applications," Gerard Smit et al. present their work on DRAs which are especially suited to streaming digital signal processing applications. In the fifth paper, "A high-end real-time digital film processing reconfigurable platform," Sven Heithecker et al. present a specialised DRA platform for high-performance digital image processing.

Future widespread adoption of DRA technology is likely to depend on both computational and communications capabilities of DRA systems. In the sixth paper, "Examining the viability of FPGA supercomputing," S. Craven and P. Athanas analyse how FPGAs' computational ability compares with traditional processors, particularly in the domain of supercomputing applications. In the final paper, "Characterization

of a reconfigurable free-space optical channel for embedded computer applications with experimental validation using rapid prototyping technology," Rafael Gil-Otero et al. investigate optical technologies which will provide future DRAs with high-speed communication abilities to match their enormous computational abilities.

Together, these papers provide an excellent snapshot of the latest research directions in dynamically reconfigurable architectures—we hope you find them useful and informative.

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