Hindawi Publishing Corporation
EURASIP Journal on Embedded Systems
Volume 2007, Article ID 27517, 1 page
doi:10.1155/2007/27517

Editorial
Embedded Digital Signal Processing Systems

Jarmo Takala,[1] Shuvra S. Bhattacharyya,[2] and Gang Qu[2]

[1] *Institute of Digital and Computer Systems, Tampere University of Technology, Korkeakoulunkatu 1, 33720 Tampere, Finland*
[2] *Department of Electrical and Computer Engineering, University of Maryland, College Park, MD 20742, USA*

Received 6 March 2007; Accepted 6 March 2007

With continuing progress in VLSI and ASIC technologies, digital signal processing (DSP) algorithms have continued to find great use in increasingly wide application areas. DSP has gained popularity also in embedded systems although these systems set challenging constraints for implementations. Embedded systems contain limited resources, thus embedded DSP systems must balance tradeoffs between the requirements on computational power and computational resources. Energy efficiency has been important in battery-powered devices, but nowadays also the limited heat dissipation in small devices calls for low-power consumption. Successful implementation of DSP applications in embedded systems requires tailoring, which in turn sets challenges for design methodologies.

For this special issue, we received 14 submissions and a collection of seven papers was finally accepted. The special issue is opened by "*Observations on power-efficiency trends in mobile communication devices*," where the authors O. Silvén and K. Jyrkkä analyze the power consumption in the current mobile communication devices. Several bottlenecks in the current implementation style have been identified, thus the paper provides a good motivation for the following papers.

In "*The Sandbridge SB3011 platform*," the authors John Glossner et al. describe a system-on-a-chip (SoC) multiprocessor targeted as a software-defined radio platform. The platform provides solutions to the challenges in future mobile devices given in the previous paper.

"*A shared memory module for asynchronous arrays of processors*" authored by Michael J. Meeuwsen et al. considers also chip multiprocessors. The presented shared memory module can be used for interprocess communication or to increase application performance by parallelizing computation.

In "*Implementing a WLAN video terminal using UML and fully automated design flow*" by Petri Kukkala et al., an automated design flow for multiprocessor SoC is presented. The flow is based on UML descriptions and the authors demonstrate their design flow with a design case.

Programming of chip multiprocessor platforms is considered in "*pn: a tool for improved derivation of process networks*" by Sven Verdoolaege et al. The paper discusses conversion of sequential programs to process networks allowing optimization of communication channels and buffers.

In "*A SystemC-based design methodology for digital signal processing systems*," the authors Christian Haubelt et al. describe a design flow for SoC designs containing automatic design space exploration, performance evaluation, and automatic platform-based system generation. The design flow is based on SystemC descriptions and the presented tools can automatically detect the underlying model of computation.

Application-specific implementations are often used to speedup certain DSP tasks in embedded systems. In "*Priority-based heading one detector in H.264/AVC decoding*," the authors Ke Xu et al. consider such implementations to speed up video decoding applications. The authors present a low-power decoder implementation for context-adaptive variable length coding defined in H.264 standard.

Jarmo Takala
Shuvra S. Bhattacharyya
Gang Qu