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Research Article

A Mixed-Signal Embedded Platform for Automotive Sensor Conditioning

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A mixed-signal embedded system called Intelligent Sensor InterFace (ISIF) suited to fast identify, trim, and verify an architecture to interface a given sensor is presented. This system has been developed according to a platform-based design approach, a methodology that has proved to be efficient for building complex mixed-signal embedded systems with short time-to-market. Such platform consists in a wide set of optimized high-performance analog, digital, and software intellectual property (IP) modules for various kinds of sensors. These IPs can be easily defined for fast prototyping of the interface circuit for the given sensor. Final ASIC implementation for the given sensor conditioning can be easily derived with reduced risk and short development time. Some case examples are presented to demonstrate the effectiveness and flexibility of this system.

1. Introduction

The increase of reliability and performances brought by electronic circuits in automotive industry is leading to the progressive replacement of predecessor mechanical and electromagnetic devices. The interest towards embedded systems for automotive derives from the fact that an emerging class of automotive applications, aimed to increase both safety and comfort levels in modern automobiles (such as X by Wire, Assisted Guidance, Collision Avoidance, and Cruising Control), requires gathering information coming from a huge number of sensors distributed everywhere in the car. The related issues are the increasing of wire length, hence weight and power consumption, and decreasing of reliability unless proper solutions are adopted. The development of efficient car network protocols [1] and the replacement of electronic boards with embedded systems are counteracting these effects. As these applications get more and more sophisticated, according to market trends and requirements, they need more and more accurate and reliable sensing elements. Moreover the high number of sensors (more than one hundred at present) will inevitably drive future choices on cheaper and less power consuming ones.

At present the above mentioned factors make the design of electronic systems for automotive applications a challenging task that cannot be handled by traditional methodologies. Electronic Design Automation (EDA) tools have continuously improved to face with the technology scaling down, while design productivity is still limited by current methodologies. The need of more complex electronic systems able to cope with the wide spectrum of applications, together with the time-to-market pressure and cost reduction, and also the design productivity gap have pushed the electronic industry towards the development of new design methodologies [2].

Among the main design methodologies described in literature and adopted by several microelectronics industries, the most referenced ones are the following:

(a) IP (Intellectual Property)-Design and Reuse: this approach [2, 3] allows the quick development of a complex ASIC by reusing pre-designed and pre-verified configurable blocks coming from different projects and/or IP vendors, thus saving time with respect to developing the IP from scratch.

(b) System Level Design: this solution [4, 5] is based on a high-level language such as SystemC used to describe HW/SW systems at multiple levels of abstraction and synthesis for a given technology.

(c) Platform-Based Design: this methodology [6–8] defines the design of electronic systems from concept to implementation as a sequence of different layers of abstractions (each layer can be considered as a platform). Concerning an embedded system, a platform can be defined as a set of modules, interfaces, services, and software that should be as much as possible configurable. They are built up taking into account the wide-ranging signal conditioning electronics for different sensors of modern automobiles, in a way that from such generic platform, the optimum interface for a specific sensor can be easily derived in a short time by means of system simulations, verifications, and possibly prototyping. This entails that only the required analog/digital components are integrated onto silicon, resulting in minimized area and power overheads.

The works in [9, 10] present a low-cost high-performance Universal (or Generic) Sensor Interface (USI) suited to interface different kinds of sensors in order to perform voltage, resistance, current, impedance, and frequency measurements. Other solutions, such as Universal Transducer Interface (UTI) [11, 12], allow handling the low-cost class of capacitive and amperometric sensors, often present in the field of Micro-Electro-Mechanical (MEM) devices. The work in [13] relates to a mixed signal platform including an analog front-end suitable for different kinds of sensors and a digital module composed by a core processor and additional general purpose peripherals. All the conditioning operations can be performed by the processor, but this solution is limited to sensors which do not need a complex signal conditioning. In [14] Murabayashi et al. present a sort of digital platform including a Digital-Signal-Processor, analog-to-digital and digital-to-analog converters (ADC and DAC) without basic analog signal conditioning (amplifiers, voltage/current drivers). This solution is limited to low-frequency signals and could not be suitable for sensors requiring a fair amount of conditioning operations. All these solutions have the advantage to be used for several types of sensors at the expenses of very little added external circuitry. Anyway there is the problem of sub-optimum architecture, since the flexibility of the system could result in area increasing, higher power consumption, and lower performances.

In this paper a platform-based methodology and a mixed-signal embedded platform for automotive sensor conditioning, developed in order to overcome the Universal Sensor Interface limitations and reduce time-to-market, are presented. The proposed solution allows to fast identifying the most appropriate architecture to interface a given sensor, to verify and to trim the overall system on a prototyping board before final ASIC implementation. The system is composed by an analog front-end, a digital DSP section, and a CPU core with peripherals.

The paper is structured as follows: after this introduction, in the next section an overview of requirements for automotive electronic sensor interface is outlined. Section 3 describes the platform-based design flow exploited to implement the mixed-signal embedded platform depicted in Section 4. Section 5 describes three case studies useful to demonstrate the versatility of the platform presented in Section 4 versus different kinds of sensors. Finally results and conclusions are drawn in Section 6.

2. Automotive Electronic Sensor Interface Requirements

A typical automotive embedded system gathers environmental data through a set of sensors, processes the data, and eventually reacts through a set of actuators. Since the cost of an electronic system involving a sensor is mainly due to the sensor itself and to its conditioning analog circuitry (for thermal compensation, dispersion of characteristics, and external environment influence minimization), the basic idea behind the considered platform is to reduce this cost by using low-price and low-performance sensors and by adding digital computational power in order to meet overall sensor performance. For this purpose, a proper digital conditioning circuitry has to be identified, trimmed, and verified in a reasonable time and early performance evaluations have to be extracted before going on towards the final ASIC product. The resulting prototyping environment is composed by hardware blocks (plugged on a prototyping board) and software facilities suitable for the design phase, while a proper verification methodology guarantees the correct system behavior. The hardware side of the platform can be identified after an investigation on the most common architectures adopted to interface a generic automotive sensor. This is examined in the following paragraphs.

2.1. Sensor Circuitry: Analysis of the Related Architectures. More than a hundred of sensors are present in modern cars [15]. They are spread along the powertrain, chassis, and body sub-systems. Among all of them, the main percentage is related to the following:

(a) powertrain: pressure, temperature, rotational motion and, recently, cylinder pressure, and rotary position for the powertrain system;

(b) chassis: chassis pressure, rotational motion, inertial acceleration, angular-rate and, recently, yaw angular rate, and steering wheel angular position for the chassis system;

(c) no absolute predominance of a particular sensor exists for the body system: the sensors are uniformly distributed among crash-sensing accelerometers, infrared thermal imaging, ambient-air electrochemical gas, and recently night-vision sensors.

The flexibility of the platform with respect to most of the above mentioned sensors can be achieved by means of a digital signal processing section: the latter includes all the required blocks to address the specific sensor requirements. In this way, whatever conditioning circuitry can be quickly mapped onto this general-purpose structure by using the hardware configuration tool. For this purpose, several conditioning circuitries have been investigated and the related digital signal processing structure has been extracted.

2.2. Temperature Sensor Conditioning Circuitry. Many sensing applications based on physical, mechanical, and chemical phenomena show an undesired thermal cross-sensitivity. These temperature influences cannot be easily shielded, and consequently, they must be measured and compensated. For this purpose, accurate temperature information has to be acquired by a temperature sensor, usually having a low impact on the cost of the whole system. Automotive applications involve temperature sensors built by means of different technologies (silicon, thermistor, and platinum film represent some examples). Suited conditioning circuitries can provide an electrical signal whose amplitude (voltage), duty-cycle, or frequency is a linear measure of the temperature. Usually the signal conditioning related to temperature sensors is always performed without using any digital circuitry. Few examples are reported in Table 1.

2.3. Pressure Sensor Conditioning Circuitry. The pressure sensor is intended for converting measured physical value (pressure) into an electrical signal whose amplitude (voltage) or frequency is a function of the applied pressure. Many principles have been adopted in order to convert the physical effect in an electrical one: to name but a few, it is possible to find capacitive, piezoresistive, and resonant effects. A proper conditioning circuitry can then associate the pressure information either to the amplitude or to the frequency of the electrical signal. Table 2 gives a list of few implementations of pressure transducers with their related conditioning circuitry, partitioned between analog and digital whenever this occurs. This short analysis reveals that the basic blocks required by the analog sensor interface are represented by amplifiers and current sources. Voltage controlled oscillators (VCOs) are used whenever frequency conversions are required or resonant conditions have to be maintained (in this case the VCO is included within a phase-locked-loop or PLL). As far as the digital section is concerned, a microcontroller can perform linearization, offset, and temperature compensation, without the use of a dedicated hardware since the bandwidth of the signal provided by nonresonant sensors is in the range 0–300 Hz.

2.4. Angular and Linear Position Sensor Conditioning Circuitry. Angular and linear position sensors are widely used for many automotive measurements and applications such as pedal position, throttle valve position, camshaft angle, transmission control, and active suspension damper systems. All of them require high resolution and high accuracy since they represent the first step of more complex and advanced control systems (e.g., Anti-Blocking-System (ABS)). The position sensors for automotive are separated in two classes: contact sensors based on potentiometric effect and contactless sensors based on magnetoresistive or Hall Effect. The former is interesting for the low cost but actually it is progressively replaced by the latter, even though a more complex digital system is required to get a linear response. Table 3 reports both industrial and research solutions to interface position sensors. The bandwidth of the signal provided by the sensor is usually limited to hundreds of Hz. Almost all position sensors are used in Wheatstone bridge configuration, and so the signal conditioning needs a differential amplifier before the ADC converter. The microcontroller unit processes the digital samples coming from the ADC block to obtain a ratiometric response of the sensor and to compensate the thermal drift of the characteristic.

2.5. Angular Rate Sensor Conditioning Circuitry. Rate sensors involved in automotive applications are mostly based on a gyroscopic structure; so they are often referred as gyro sensors; they provide an output voltage proportional to the angular rate of the vehicle, thus allowing the sensor to be used in applications such as chassis suspension control (vehicle roll and pitch), vehicle stability, and vehicle-heading navigation (yaw). Implementations of a rate sensor by using a gyro require a discrete amount of conditioning circuitry since the rate information is associated to the vibration, which has to be maintained and controlled for the sensing element at different operating conditions (temperature changes, shocks, etc.). Table 4 lists different conditioning circuitries for the considered type of sensor. Interfaces for this kind of sensor usually share the same conditioning circuitry for sense (a cascade of amplifier, demodulator and filter), for driving (PLL and automatic gain control AGC), and balancing (gain, offset adjustment).

2.6. Acceleration Sensor Conditioning Circuitry. The acceleration sensor is intended for converting the measured acceleration into an electrical signal. Table 5 reports different conditioning circuitries for the considered type of acceleration sensors. These sensors are used in the automotive field for vehicle dynamic control and suspension control applications or as shock/vibration sensors to detect collisions or forced intrusion into the car. Moreover they can be used as tilt sensors to detect if a vehicle is being jacked up, about to be towed, or being loaded onto a flatbed truck, that are some of the most common methods of car theft today.

All information extracted from previous sections can be summarized in the following considerations: most of the sensors share a basic group of analog blocks represented by amplifiers and current and/or voltage sources. Since we are interested in moving the remaining conditioning circuitry to the digital side (for cost, flexibility, and prototyping reasons), DAC and ADC blocks are required to interface the analog and the digital domains. This allows building the digital side of the platform in a configurable structure, made-up by all possible blocks required to complete the sensor signal conditioning chain and to customize it for the considered sensor. High configurability is needed for the analog section to be able to acquire voltages and currents or to perform

Table 1: Examples of temperature transducer conditioning circuitry.

Technology	Input/output	Analog circuitry	Digital circuitry
Silicon [16]	temperature/frequency	PTAT, ring-oscillator, pulse generator, divisor	
Silicon [17]	temperature/voltage	lock-in amplifier, lowpass filter	
Silicon [18]	temperature/voltage	PTAT, comparator, DAC	shift-register for the threshold
Silicon [19]	temperature/voltage	PTAT, bandgap, chopper amplifier, sigma-delta converter	I^2C interface
Thermistor [20]	temperature/voltage	Wheatstone bridge, amplifier	

Table 2: Examples of pressure transducer conditioning circuitry.

Effect	Input/output	Analog circuitry	Digital circuitry
Capacitive [21]	pressure/voltage	operational amplifier, filter, ADC, analog multiplexer	counter, decoder
Piezoresistive [22]	pressure/frequency	transconductance amplifiers, sigma-delta converter, compensation resistors, band-gap	
Piezoresistive [23]	pressure/voltage	Wheatstone Bridge, Schmitt trigger	microcontroller
Piezoresistive polysilicon-on-steel [24]	pressure/voltage	operational amplifiers, DAC	registers for various compensation and calibration during manufacturing
Capacitive [25]	pressure/voltage	analog multiplexer, ΣΔ modulator	FPGA, USB interface
Capacitive [26]	pressure/voltage	operational amplifier	microcontroller (with ADCs and peripherals) for linearization, compensation and calibration
Resonant (by thermal excitation) [27]	pressure/frequency	piezoresistive element for vibration sensing (SR510 lock-in amplifier)	(SR510 lock-in amplifier)

capacitance and resistance measurements. The digital part has to be able to elaborate the data coming from the analog section and to perform the signal processing that cannot be done in the analog side.

3. Platform-Based Design Flow

The starting point of our approach is based on the realization of a MATLAB model for the system at the highest abstraction level, which is made of a set of functional blocks with no distinction between analog/digital sections and software. The sensor itself can be modeled with MATLAB and thus co-simulated with the conditioning circuitry, helping the designer find the most appropriate conditioning chain for the given application. A system exploration phase, based on simulations, design iterations, and functional blocks refinements, leads to a first partitioning of the system in analog, hardwired, and programmable (software) digital building blocks. Although this subdivision cannot be taken as frozen, the accurate MATLAB modeling and simulations guarantee the validity of these choices.

Then each block is modeled with the most appropriate description language: VHDL for digital hardware, VHDL-AMS for analog circuitry, and C/C++ for software routines. The top-down platform-based design flow is depicted in Figure 1: from the initial behavioral model we get to lower levels of abstraction via synthesis steps. The result of a synthesis step is then validated with the previous one through a verification phase. Concerning the digital section, a Gate-Level VHDL is realized for the selected technology exploiting a Register Transfer Level (RTL) description and a synthesis tool.

On the analog side, starting from VHDL-AMS (modeling no more than the specifications), a transistor-level description is generated, from which a more accurate VHDL-AMS model can be obtained and employed in a mixed-signal simulation, together with standard VHDL and C software running on the programmable hardware (microcontroller or general purpose processor). After the implementation of each single block, the relevant behavioral model is updated, so that it behaves closer to the practical circuit. This feedback process increases mixed simulations efficiency, allowing a more comprehensive design space exploration and reducing the probability of system architecture re-design [2]. VHDL-AMS becomes therefore crucial to let designers simulate the whole system during its own development, compare

Table 3: Examples of angular and linear position sensor conditioning circuitry.

Type	Input/output	Analog circuitry	Digital circuitry
Anisotropic MagnetoResistive (AMR) [28]	angle or displacement/voltage	amplifiers, ΣΔ converter, oscillators, comparator, voltage reference,	decimation filter, ALU, SPI interface
AMR [29]	angle or displacement/voltage	differential amplifiers, lowpass filter, ADC/DAC converter, current amplifier	microcontroller for calibration, compensation and linearization
lateral MagnetoTransistor [30]	angle/bit stream	differential amplifier, incremental ADC, adder, DAC converter	microcontroller
Hall Effect [31]	linear displacement/voltage	low noise instrumentation amplifier	
inductive attenuating coupler [32]	angle/duty-cycle	amplifiers, multiplier, IF filter, lowpass filter, comparator.	digital signal generator
AMR [33]	linear displacement/voltage	analog multiplexer, differential amplifier, ADC/DAC converter, voltage reference	Microcontroller for calculating the position

Table 4: Examples of rate transducer conditioning circuitry.

Type	Input/output	Analog circuitry	Digital circuitry
piezoresistive composite beam [34]	angular rate/voltage (open loop)	sine generator, multiplier, lowpass filter, amplifier, AGC	
tuning fork quartz [35]	angular rate/voltage (open loop)	differential amplifier, lowpass filter, AGC, synchronization blocks	
bulk silicon [36]	angular rate/digital	ΣΔ ADC, PLL, AGC DAC charge, phase shifter, charge pump	I/Q demodulator, DSP for calibration and compensation
vibrating mass [37]	angular rate/digital	C/V converter, ΔΣ modulator, PLL, AGC, temperature sensor	
vibrating mass [38]	angular rate/voltage	C/V converter, AGC, phase shifter, filters, demodulators (separated control and sense electronics)	

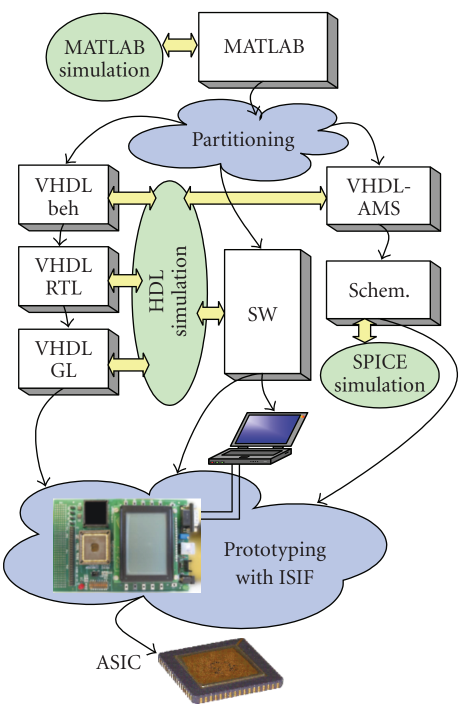


Figure 1: Platform-Based Design Flow.

results with those given by MATLAB, and thus be able to fix as soon as possible unexpected behaviors, by trimming the architecture and updating blocks functionalities or specifications. The above mentioned design flow ends up with the prototyping phase, through which the whole system can be tested (or parts of it) under practical operating conditions [39, 40].

The platform-Based Design flow guarantees two main advantages: on one side this methodology represents a powerful strategy for managing complex designs within short time-to-market as it is typical of aggressive industrial applications. This is obtained by high reuse of concepts, architectures, blocks, and IPs among different projects thanks to the multi-abstraction-layer design. On the other side, the strong customization on the target application of the lower abstraction layers is essential to achieve top performances, unreachable with generic multi-purpose designs. As a matter of fact system design space exploration for sensor conditioning architecture definition only by high-level simulations is critical. In this case the system has to be modeled together with the target sensor in order to get the best possible architecture for the conditioning sensor interface. This may imply several design iterations from the prototype back to the abstract level (thus slowing

Table 5: Examples of acceleration transducer conditioning circuitry.

Effect	Input/output	Analog circuitry	Digital circuitry
Capacitive [41]	acceleration/voltage	demodulator, switched capacitor filter, amplifier with programmable offset	Digital calibration of amplifiers
Capacitive [42]	acceleration/digital	charge amplifier, Sample&Hold, comparator, ΣΔ modulator	
Capacitive [43]	acceleration/voltage	dual Chopper amplifier, demodulator	
Resistive [44]	acceleration/voltage	amplifier	
resonant beams [45]	acceleration/voltage	oscillator, Automatic Amplitude Control, switched-capacitor amplifier, filter	
Piezoresistive [46]	acceleration/voltage	sample&hold, Bandpass filter, rectifier, averaging stage	

the time-to-market), not due to design faults but only to unavoidable mismatches between a high-level modeling and physical reality. The main consequence is that these small inaccuracies might result in final wrong conditioning chain implementation and in poor specifications for critical blocks. These design issues can bring to a final prototype affected by significant design inaccuracy leading to necessary re-design cycles with a consequent increase of costs and time-to-market inflation. Another big question mark for system engineers stays in specification definition, estimation of final system performances, and, in the end, decision whether the project is feasible or not: a MATLAB simulation can hardly give enough information of this kind.

3.1. Design Flow Based on ISIF Embedded Platform. The most important advantage of the ISIF design flow is represented by the drastic reduction of the time needed to perform the design architectural space exploration. In place of time-consuming simulations, with ISIF the application can be directly evaluated on the real silicon (thus a prototype of the target application is possible before its actual design). Furthermore accurate feedback information coming from IPs already on silicon can be of crucial importance, since phenomena impossible to be foreseen in a traditional design simulation can be observed. In addition a correct evaluation of the real parasitics can be developed thus allowing designers to reach a very accurate estimation of the performance of the device to meet the specification of the final product.

Although ISIF presents some similarities with the Universal Sensor Interface (as it aims to condition a wide class of sensors) [9, 10], it should not be considered a final product for any target application. Indeed, its aim is to provide designers with a powerful and complete interface for a quick development of a final product with reduced risks and short development time in order to achieve the highest performances and the lowest overheads. This fact entails that only the required analog/digital IP components are integrated onto the final silicon for production, resulting in minimized area and power overheads.

As soon as the sensor is available we could connect directly the ISIF platform. The architecture space exploration can be rapidly started by simple acquiring the signal by an analog conditioning channel, trimming the signal conditioning path with the desired analog IPs and then apply complex and ad hoc algorithms thanks to the hardware DSP structure and the emulation of software IPs. After the ISIF system exploration phase, the Platform-Based Flow can start straight from the HDL development of the software-emulated IPs, with a noteworthy saving of design space exploration time and a reasonable confidence in architecture goodness and clear expectation of system final performances. As soon as the prototyping phase has been successful completed all the necessary analog, digital, and software modules have been identified with relevant interconnections. Starting from this result the final ASIC in the same technology could be easily achieved with short development time and, above all, with very low development risk.

ISIF platform, which is described in detail in Section 4, has been primarily studied to provide interfacing for capacitive and resistive sensors, to perform measurements of voltages and low currents and many other applications [47].

4. ISIF Platform

The ISIF platform provides a set of high-performances programmable analog and digital IPs directly on silicon and it is able to configure their interconnections and integrate them with DSP software routines. These routines emulate hardware blocks and/or are used to perform calibrations and compensations. Figure 2 gives an overview of the main ISIF sections: an analog front-end, a digital DSP section, and a CPU core with peripherals. Moreover, all the analog and digital IPs are fully programmable by a set of status registers linked together in a serial JTAG-like chain. For these reasons, different interfacing architectures, data paths, and signal processing chains can be quickly implemented and evaluated on the field allowing a fast and flexible interfacing, characterization, and test of the sensor.

ISIF platform has been implemented in 0.35 μm Bipolar CMOS DMOS technology supplied by STMicroelectronics, on a single chip with area occupation of about 72 mm^2 (Figure 3).

4.1. Analog Section. The ISIF analog section consists of a set of programmable IPs for signal acquisition and basic

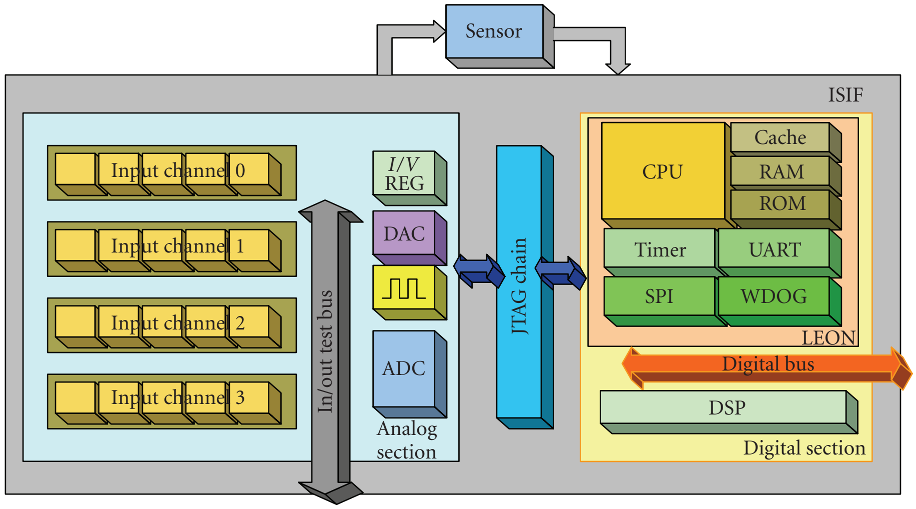
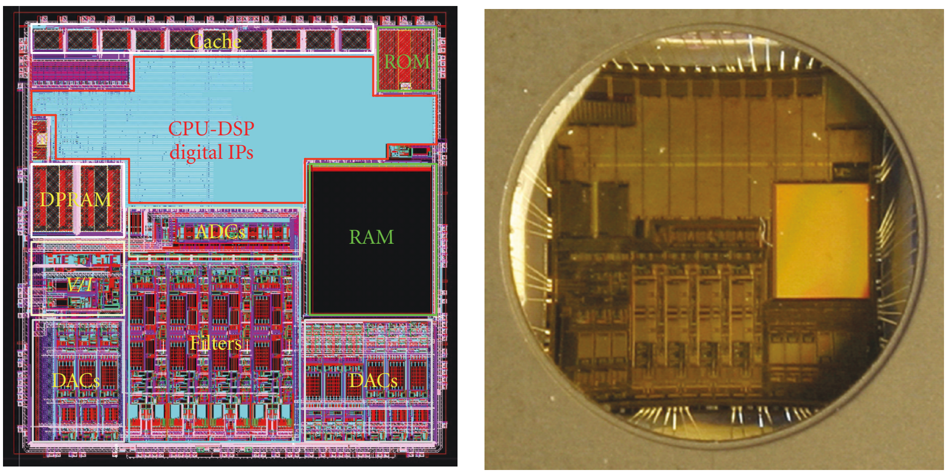


Figure 2: ISIF Platform architecture.



(a) (b)

Figure 3: ISIF layout and chip photo.

conditioning such as DACs, ADCs, amplifiers, filters, and voltage/current sources.

ISIF analog section features 4 dedicated input channels for sensor signal acquisition (Figure 4). The readout stage is realized recurring to an operational amplifier that can be programmed to implement a charge amplifier, a trans-resistive stage, or an instrument amplifier thus covering a wide range of sensor typologies. The following signal analog processing is realized recurring to fully differential stages that perform signal recovery, by means of highly configurable amplifiers, and lowpass filters for antialiasing purpose. Then the signal is converted by a fully differential 12-bit ADC or a 16-bit ΣΔ ADC. Voltage and current references are all derived by a low-noise bandgap reference and they are trimmable in order to achieve the required specifications in terms of noise and power consumption. The sensor driving stage of the platform is provided by a set of configurable 12-bit and 10-bit thermometer DACs. An input/output analog test bus can be driven to supply external stimuli or to probe output signals at each block output, guaranteeing an effective and quick way to debug the analog signal conditioning path.

The analog section has been developed keeping the design philosophy as near as possible to the digital counterpart: high configurability of blocks and signal paths and design for testability and reliability are unquestionably welcome in every design but are often hard to be matched with excellent performances (up to the automotive standards). For example, a high number of configuration bits can easily lead to an increase of parasitics and noise due to routing lines extension and digital switches slew (to give an idea, the four ISIF input channels with 7 bypassable stages each feature about 1000 configuration bits). The above mentioned problems have been overcome by using separate power supplies and grounds for digital (3.3 V) and analog (5 V) sections, provided by independent regulators, thus improving noise margin. System routing has been eased and automated employing modular outline of analog blocks. Programmability of IP cells has been carried out by means of a JTAG-like serial chain which minimizes routing complexity of configuration lines.

4.2. Digital Section. Digital section is involved both on processing and monitoring activities. CPU block (Figure 5) includes a LEON core with related peripherals and dedicated IPs for DSP purpose. The LEON is a general purpose processor based on a 32-bit RISC Scalable Processor ARChitecture (SPARC-V8) compliant architecture designed for embedded applications. The LEON processor is developed by the European Space Agency and freely distributed under Lesser General Public License [48]. The LEON comes with several features on-chip such as hardware multipliers, dividers, interrupt controller, memories, an AMBA bus bridge, and peripherals for external communication.

The digital section features a dedicated hardware digital signal processing unit, composed by fully configurable IPs optimized for low power consumption such as modulator and channel demodulators, a 6 DAC controllers, filters (FIR and IIR), and a sine wave generator which can provide up to 16 waves with 3 different frequencies and programmable phases. These IPs feature a flexible interconnection architecture: they are hardware interconnected but they can also be accessed at their input/output by software. LEON processor features system monitoring and controls signal processing chain and communication with external devices. The digital section is completed by standard peripherals such as timers, watchdog, SPIs (Serial Peripheral Interface), UARTs (Universal Asynchronous Receiver Transmitter), CACHE, ROM RAM, and EEPROM memories (Figure 5). Part of the software is included in the ROM (boot and few utility functions), while the rest can be downloaded at startup via UART or can be stored in external SPI EEPROM and so directly reboot from EEPROM (which can hold different software and data for speed up time in trimming and test procedures). Firmware utilities can change interconnections among digital IPs, handle communications with external devices (for debug, monitoring), and configure the whole analog front-end section (changing parameters such as gain, bandwidth) to match requirements of different sensors.

4.3. DSP Software Section. The requirements of automotive applications are pushing towards the use of hardware solutions (especially concerning safety issues). On the other hand the high number of variables (e.g., regarding block and datapaths dimensioning) makes hardware implementation very difficult to be successful at first time. Furthermore several digital IPs require detailed analysis for proper parameters setting since automotive applications often require both high performances and reduced area, aspects not compatible with the use of a large number of configuration bits for trimming or over-dimensioned paths. To meet these requirements, the ISIF platform includes software peripherals (e.g., filters, controllers) characterized by a perfect functional match with hardware devices.

The LEON CPU guarantees the required computational power for real-time software IPs implementation thanks to good signal processing features (hardware multipliers and accumulators). Therefore all functionalities, which are not fulfilled by ISIF digital section, can be emulated by software routines keeping the same behavior of the original DSP library IPs (concerning bits width, saturation, linearity, etc.).

This feature allows input/output data to be acquired from digital IPs, then a series of DSP routines can be called, and eventually the results can be passed back to physical blocks just as the data elaboration would have been realized completely by hardware IPs. An example of hardware/software mixed architecture is shown in Figure 6. The monitoring, control, and communication functionalities are implemented via software with two main benefits: flexibility and possibility of updating due to system modifications and new specifications. These features lead the designer to identify the most suitable solution in DSP elaboration for a specific sensor. In the final ASIC design, all the DSP software routines (and even the LEON processor which is quite area and power consuming) can be replaced with hardware IPs with a zero risk for redesign, drastically reducing time-to-market. The designer can change analog settings and interconnections of digital IPs and even instantiate new ones with a Personal Computer connected via UART to the ISIF board. This allows a rapid and effective design architecture exploration in order to achieve architecture optimization both in terms of area and performances. The whole analysis can be developed from the beginning of the interface concept with the sensor connected to the ISIF board.

4.4. Graphical User Interface. Analog test buses and registers are programmable by means of a JTAG-like chain accessible via LEON processor or directly from outside through four dedicated pins. To avoid any mistake in setting the JTAG-chain (the JTAG configuration includes hundreds of bits for each IP and a manual configuration of each bit would be quite difficult) a dedicated LABVIEW Graphical User Interface (GUI) has been developed. This interface can download the firmware containing the target JTAG and registers' settings directly on chip through the UART. Once the configuration of ISIF has been set by the user-friendly GUI, the LABVIEW software generates a text file with the settings of all the analog and digital IPs. The text file is then used by the LEON firmware compiler and the settings are taken as parameters for the configuration chains of the different IPs. The GUI is able to apply minor changes to the configuration of all IPs' settings at run-time as well. This type of configuration is exploited mainly when minor run-time changes of the configuration are needed. A firmware module running in the LEON firmware implements a communication protocol with the LABVIEW software running in the Personal Computer. Following this protocol, the GUI is able to set each IP's configuration register. The GUI is depicted in Figure 7 where the configuration of a 12-bit DAC is taken as an example.

5. Test Cases

As already pointed out in the previous section, ISIF is an extremely versatile platform suitable to address many

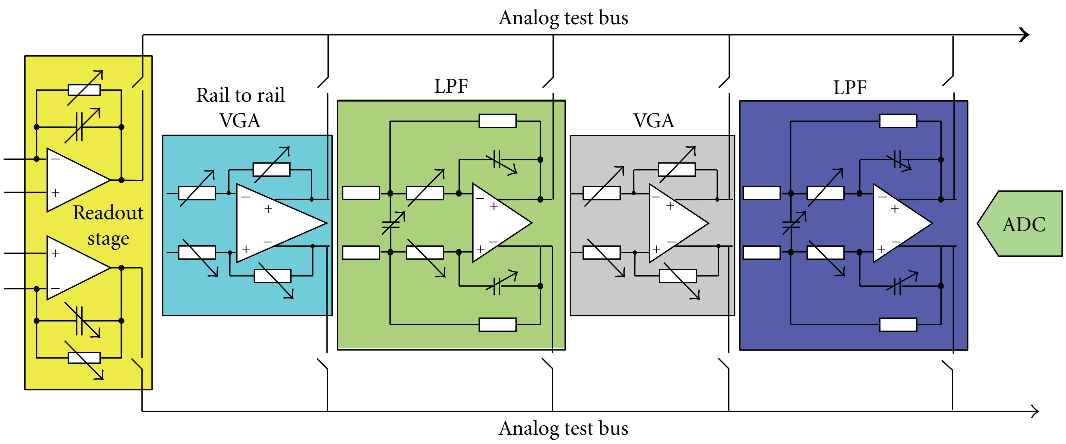


Figure 4: Input channel block diagram.

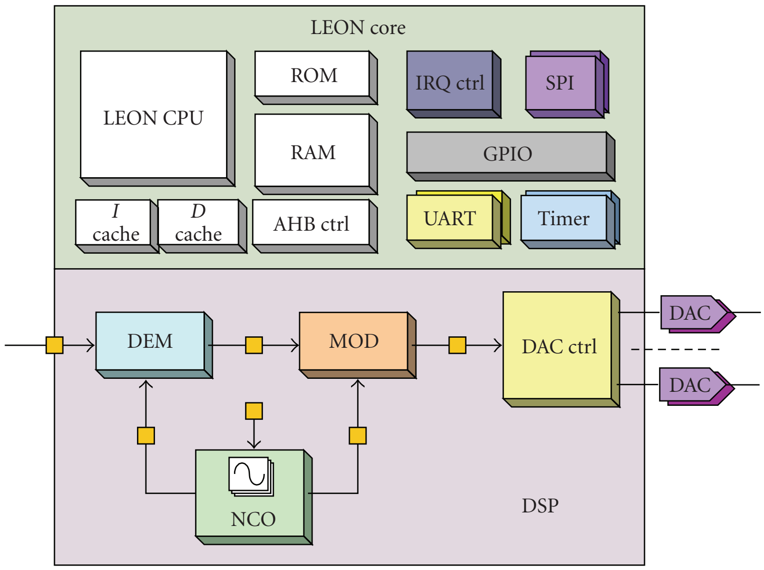


Figure 5: LEON and Digital hardware IPs.

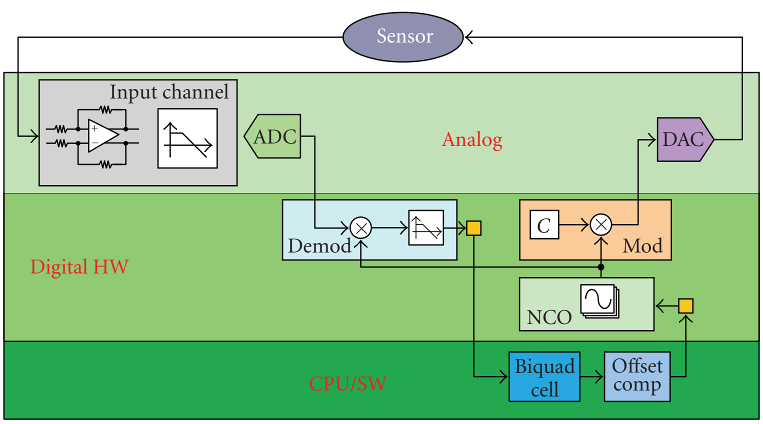


Figure 6: Example of a mixed analog, digital hardware, and software DSP architecture implemented by ISIF.

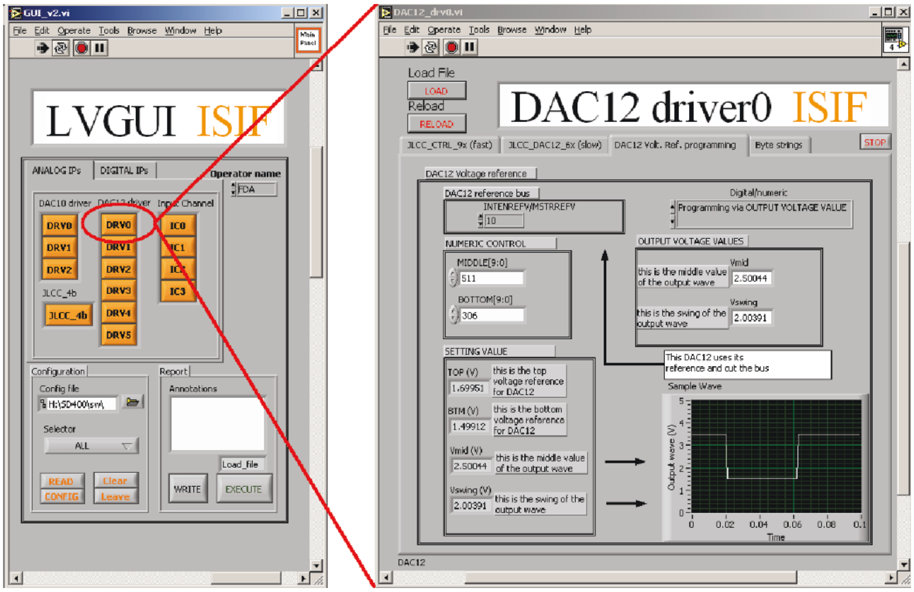


Figure 7: LABVIEW GUI.

different sensors with a short set-up time, thanks to its high configurability of both analog and digital hardware and the powerful software resources made available by LEON core. Yet ISIF can be configured for prototyping many kinds of sensor interfaces, like accelerometers, magnetosensors, gyrosensors, and so on, with low effort, low cost, and short set-up time. We would like here to better point out these features with regard to three different test cases: Magnetic angular position sensor, Low-*g* Accelerometer, and Rate Gyro Sensor.

5.1. Magnetic Angular Position Sensor. Magnetic sensors have a wide range of applications such as proximity detection, displacement sensing, rotational reference detection, and current sensing. The considered angular position sensor is based on magnetoresistive (MR) effect and represents a robust, precise, and also cost-effective solution for angular measurements in the harsh automotive environment. An MR sensor [28] exploits the physical properties of a thin strip of a certain ferromagnetic alloy in which the electrical resistance is a function of the magnitude and of the direction of an external magnetic field. In particular, if the magnitude of the external magnetic field is greater than approximately 6 KA/m (called saturated field), the resistance of the MR becomes sensitive only to the direction of the field itself. This condition is applied whenever angular measurements rather than field measurement have to be performed.

If θ is the angle between external saturating magnetic field M and the current I flowing into the MR (Figure 8(a)), the resistance of MR itself is given by the expression (1):

$$R = R_0 + \Delta R_0 \cos^2\theta. \tag{1}$$

When four MR sensors are arranged in a Wheatstone bridge configuration (Figure 8(b)), the differential output signal available on the diagonal of the bridge is given by (2):

$$V_0^+ - V_0^- = V_{\mathrm{dd}} \cdot S \cdot \sin(2\theta), \tag{2}$$

where S (typically 15 mV/V) is the sensitivity of a single MR. Expression (2) shows dependence from the supply voltage V_{dd} and from the sensor sensitivity S, the latter being a function also of the temperature T. The sensor is applied to a mechanical system (Figure 8(c)), composed by a permanent magnet of disc shape (for saturating the MR sensors) coaxially to a rotary shaft, whose angular position has to be measured. The shaft can turn around its axis for an angle of 90°; so the differential output from the sensor is limited to the sinusoidal curve within the dashed box in Figure 8(d). This is also the maximum range for which no uncertainty occurs.

Theoretically, to produce a linear response from the signal gathered from the sensor, an inverse sine function could be applied; in practice, either for nonlinearity reasons or from drops on the supply voltage and/or temperature fluctuations, it is preferable to store in a ROM memory the sensor characteristic (voltage versus angular position) for a standard condition and to correct it whenever the conditions change. For this purpose, the platform can be used to make all the operations required.

For this application two ISIF input channels have been configured for instrument amplifier voltage detection (Figure 9). Analog data have been converted and digitally processed by DSP software routines, while LEON forwards output data (via UART) to a host PC for screen displaying and postprocessing. To compensate the dependency of the Wheatstone bridge signal from the temperature, a thermistor is used. In this way the processor can control the gain of the bridge amplifier as a digital feedback loop improving the overall system accuracy. The measured sensitivity amounts to 0.1°/s with signal up to 10 KHz bandwidth.

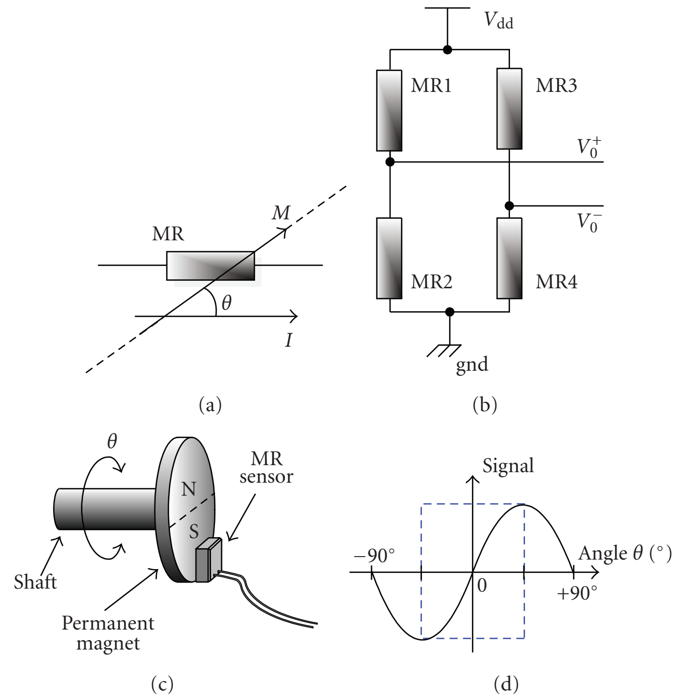


Figure 8: MR resistor with magnetic field (a), related Wheatstone bridge configuration (b), angular position sensing solution (c), and related output characteristic (d).

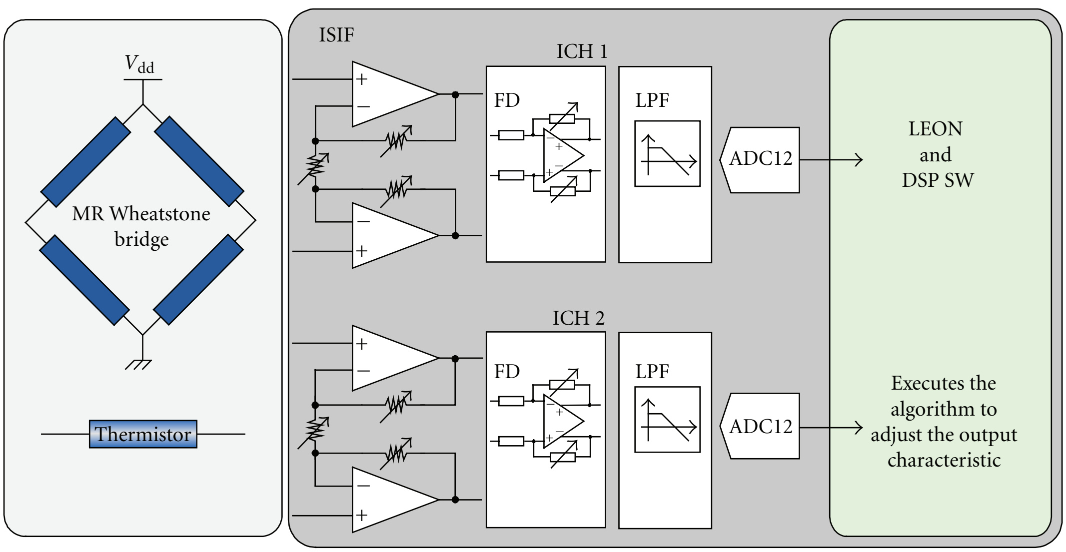


Figure 9: Angular sensor conditioning circuitry.

5.2. Low-g Accelerometer. Low-*g* micromachined capacitive accelerometers are commercially successful inertial sensors. There are many different types of capacitive accelerometers but their basic structures are very similar. They typically consist of a proof mass suspended by beams anchored to a fixed frame [49]. The presence of an external acceleration displaces the support frame relative to the proof mass, thus changing the capacitance between the proof mass itself and a fixed conductive electrode separated from it with a narrow gap. This technique is carried out using two main basic structures: the vertical and the lateral ones. In the vertical structure the proof mass is separated by a narrow air gap from a fixed plate, forming a parallel plate sense capacitance. In this case the sense direction is perpendicular to the proof mass plane (z-axis). In a lateral accelerometer, fingers extending from the proof mass (sense fingers) are interdigitated with fixed fingers, forming parallel differential capacitor elements. In these devices the proof mass moves along its plane as shown in Figure 10 ($x - y$ plane).

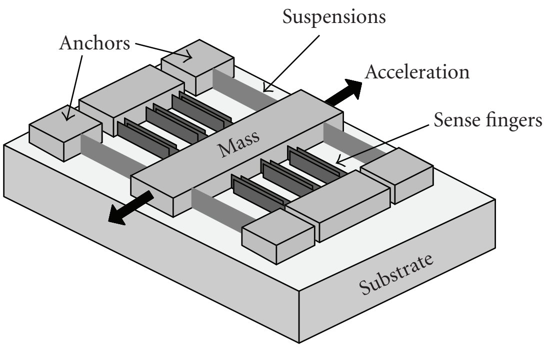


Figure 10: Low-g micromachined capacitive accelerometer.

Readout circuits mostly use capacitance-to-frequency converters [50, 51], capacitive AC-bridges [52], or switched capacitor circuits [53, 54]. Sometimes switched capacitor circuits are exploited to implement the correlated double-sampling (CDS) technique in order to reduce the effect of $1/f$ noise [54, 55]. Moreover accelerometers can be operated open loop or closed loop. The open-loop solutions are inherently stable and they require simpler circuitry but the linearity, bandwidth, and dynamic range cannot be better than the sensor itself. The closed-loop solutions improve these performances at the cost of a more complex circuitry and risks of instability.

In this section an ISIF implementation with YZ dual axis accelerometer is described. Such accelerometer features an in-plain moving structure which shifts on Y axis when subject to an acceleration, causing a ΔC variation of about 10 fF/g in the sense capacitances, whose rest value is about 10 pF. The Z moving structure is subject to a torque under acceleration, thus featuring poor linearity, but is provided with feedback electrodes in order to implement a closed loop conditioning: up to ± 4 g acceleration can be compensated, making possible the closed loop architecture in the target low-g range of ± 2 g.

The slight ΔC variation in low-g applications makes necessary a differential capacitance reading provided by ISIF charge amplifier (Figure 11). The input channel stages have been configured to perform a further lowpass filtering and gain adjustment, so that the input dynamic of the 12-bit ADC converter can be fully exploited. The digital section decimates the ADC output and lowpass filters, while software-emulated IPs complete the signal processing chain. Closed loop is implemented on Z axis by a reference subtraction, a DSP controller, and a feedback actuation, being the acceleration value calculated as the difference between feedback driver inputs. Such signal requires further filtering (down to the target bandwidth of 10 Hz), offset compensation, and gain correction in order to have the chosen sensitivity. Signal coming from Y axis (open loop) is directly fed through lowpass filters and offset/gain correction stages. Comprehensive studies on the influence of temperature (T) on the combination of sensor and interface have revealed an almost linear trend of offset and sensitivity over T. For this reason a software T drift linear compensation has been set up, including ISIF temperature sensor readout, lowpass filtering, and measured T employment for calculating offset and gain correction additional coefficients.

The system provides digital output via UART or SPI, with sensitivity of 1024 LSB/g and FS of ± 2 g. The noise stays within 3 mg for both axes (with 10 Hz bandwidth). The linear procedure for compensation over T resulted in a max offset drift of 20 mg on Y and 40 mg on Z, with sensitivity error within 1% of full-scale (FS) on Y and 3% of FS on Z [56]. With respect to commercial devices [57], this implementation features a slightly higher noise but better 0 g offset and stability over temperature.

5.3. Rate Gyro Sensor. Gyro sensors provide yaw rate measurement by working accordingly to the Coriolis Effect [58]. The sensor is kept oscillating at its proper resonant frequency by a driving sine wave signal supplied to two sensor electrodes; so an angular rotation of the MEMS causes a perpendicular oscillation. This induced oscillation can be discriminated by detecting the capacitance variation at the sensing electrodes. For such application the electronic interface has to provide a sine driving by a PLL (Phase-Locked Loop) with the capability of locking at the gyro resonating frequency (around 5–10 KHz); meanwhile an Automatic Gain Control (AGC) keeps its amplitude at a safe level: more driving implies better SNR, but excessive amplitude makes the moving structure hit the fixed frame and causes sensor malfunctioning. A filtering path (with gain and offset compensation) is required after demodulation for the detected rate signal. This interface can be easily implemented by ISIF platform: two analog input channels are used for signal acquisition and a preliminary filtering and dynamic conditioning; then the PLL and the AGC functionality is performed by the hardware modulator, demodulator, and the NCO (Numeric Controlled Oscillator). The DSP structure, which closes the loop for implementing the PLL and ADC, is developed by means of firmware utilities: a DSP controller, generic transfer function for loop filtering, signal gain adjustments, and offset compensations (Figure 12). Gyroscope DSP firmware routine basically works on the execution of the on a time schedule given by data valid coming from hardware at about 1 KHz. The remaining time (within two interrupts) is used to handle communication resources such as UART and SPI (both can be used for sending commands and reading outputs).

The customization of the whole system for gyro sensor conditioning, including optimal input channel gains and bandwidth setting, hardware IPs configuration, and software modules setup, has been performed in roughly one week and resulted in a working system with a sensitivity of 20 mV/(°/s) and a rate noise of 0.4°/s on a 10 Hz output bandwidth. The results achieved by ISIF fast prototyping can be compared with commercial devices. Rate noise stays at higher levels due to the slightly higher parasites of the signal acquisition stage (input switch matrix and programmable R and C for charge amplifier); yet it still reaches the levels of the commercial chips from Analog Devices [59] or Murata [60] reported as a reference. The optimized interface for gyro sensor can be designed using the ISIF prototype as a starting point, reusing

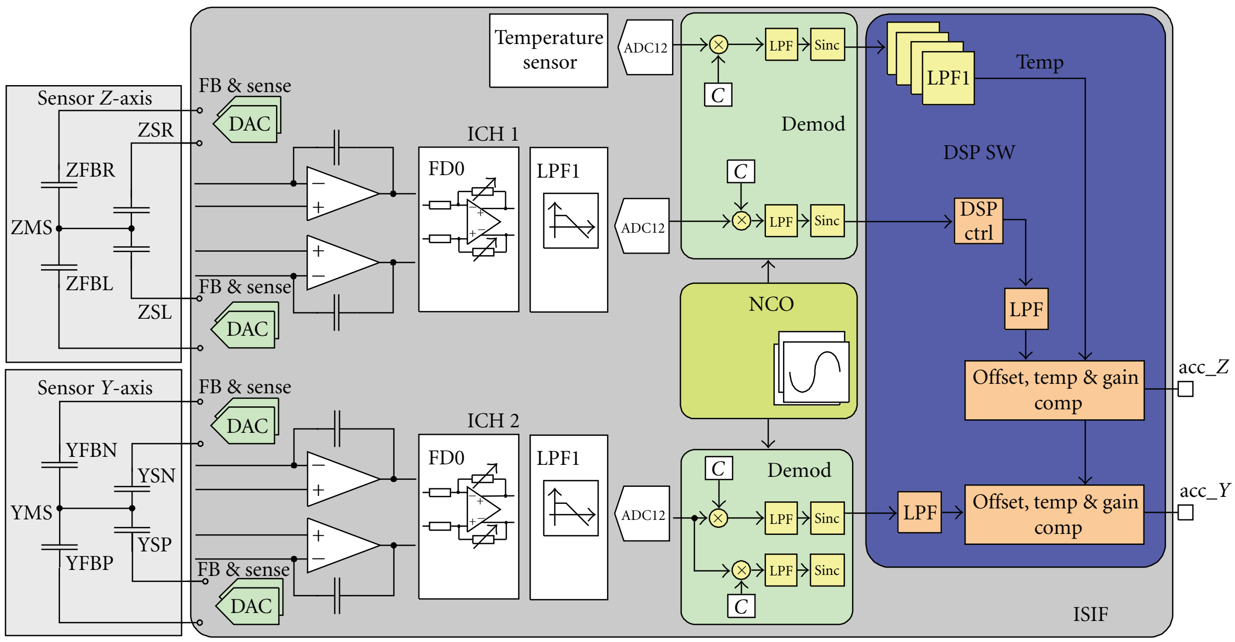


FIGURE 11: Accelerometer readout conditioning chain implemented with ISIF.

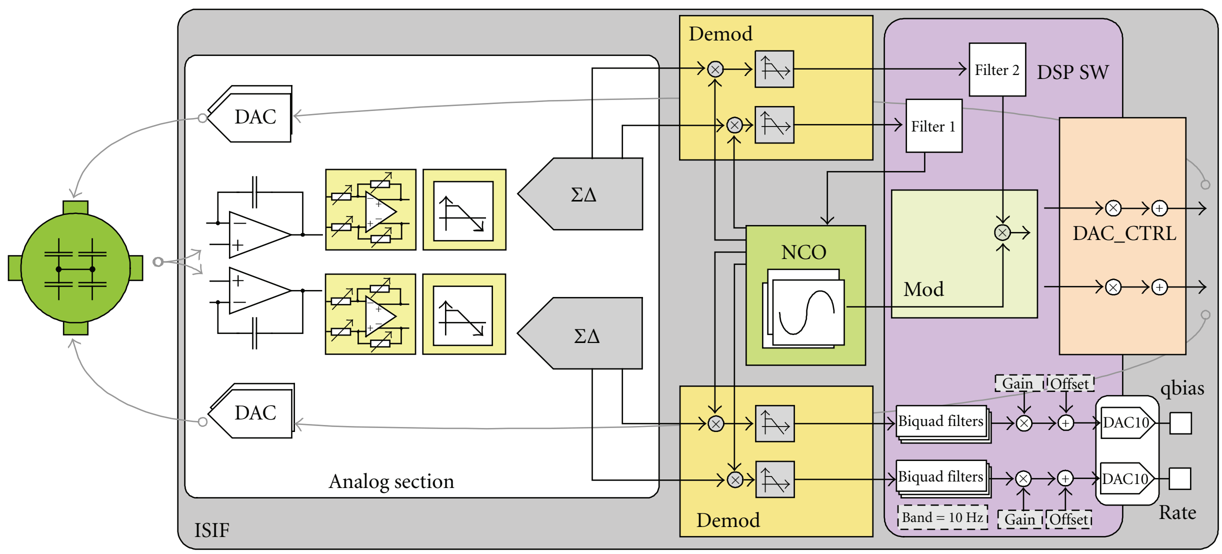


FIGURE 12: Gyroscope readout conditioning chain implemented with ISIF.

most of its blocks (simply cutting unneeded configuration options) and thus minimizing area, power consumption, and parasites, with a strong confidence in achieving a first time successful silicon with superior performances.

6. Conclusions

In this paper a platform-based design methodology which allows fastening the development of a mixed-signal embedded system to interface a given automotive sensor has been presented. The ISIF mixed-signal embedded platform has been designed to offer a wide range of software, digital, and analog IPs in order to fast identify, verify, and prototype a suitable architecture for automotive class sensor before proceeding to the final ASIC implementation.

The platform has been developed on a single chip of about 72 mm^2 using a 0.35 μm BCD (Bipolar CMOS DMOS) technology.

Three applications cases have been presented in order to demonstrate the validity of the prototyping environment and to proof its versatility towards different sensors. Obtained results, successfully compared with state-of-the-art approaches but with a very low set-up time, confirm the efficacy of this methodology.

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